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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,273	LIN, CHUN-CHIEH	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application (on 12/29/2003).

Information Disclosure Statement

It is herewith made of record that no Information Disclosure Statement has been found in the file to date.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The term "high-k dielectric material" in ***claims 23 and 48*** is a relative term, which renders the claim indefinite. The bounds of the concept "high" implicit in the term "high-k dielectric material" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

3. ***Claims 28 and 29*** recite the limitation "the interposing portion" in the respective lines 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-3, 7-8, 12, 14, 18-20, 24, 25, 56, 57*** are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al (6,040,589). Zhang et al teach a microelectronic device, comprising (see Embodiment one, col. 6, l. 55 – col. 8, l. 47): an insulator 302 (of silicon oxide, hence comprising an oxide: *claim 20*) located over a substrate 301 (col. 6, l. 60-65 and Figures 3-5, particularly Figure 5C); a semiconductor feature 303 (col. 6, l. 62-67) located over the insulator and having a thickness, a first surface opposite the insulator (its upper main surface; Figure 5C), and a sidewall spanning at least a portion of the thickness (sidewall of 303 in Figure 5C); and a contact layer (titanium substrate portion of 318 and 321) (col. 7, l. 62 – col. 8, l. 42) having a first member titanium substrate portion of 318 (loc.cit.) extending over at least a portion of the first surface (Figure 5C) and a second member 321 (loc.cit.) spanning at least a portion of the sidewall (Figure 5C).

On claim 2: a portion of the semiconductor feature interposes the insulator and the second member of the contact layer (because a straight line can be drawn from a point in the insulator to a point in the second member that intersects the semiconductor feature).

On claim 3: the portion of the semiconductor feature interposing the insulator and the second member of the contact layer has a thickness of at least 50 Angstroms, namely 500 Angstroms (col. 6, l. 62-67).

On claim 7: the contact layer comprises metal (col. 7, l. 50-62).

On claim 8: Zhang et al teach the selection of metal silicide for said contact layer (col. 1, l. 40-47).

On claim 12: the contact layer comprises metal oxide (col. 8, l. 37-42).

On claim 14: the semiconductor feature by Zhang et al comprises silicon (col. 6, l. 66-67).

On claims 18-19: the semiconductor feature has a thickness of at least about 400 Angstroms (claim 18) and at least about 100 Angstroms (claim 19), namely 500 Angstroms (col. 6, l. 60-67).

On claim 24: the insulator comprises a buried oxide layer 302 (col. 6, l. 60-65) (302 does not reach any outer surface).

On claim 25: the substrate is a silicon-on-insulator (SOI) substrate having an insulating layer 302 interposing a semiconductor layer 303 and a bulk substrate 301, the insulator is defined in the insulating layer (silicon oxide), and the semiconductor feature (crystalline silicon) is defined in the semiconductor layer (col. 6, l. 55-67).

On claim 56: Zhang et al teach an integrated circuit device (active matrix device, for instance: see claim 15 in Zhang et al, col. 17, l. 24-45), comprising: an insulator 303 formed over a substrate 301; a plurality of microelectronic devices (TFTs) (cf. "Summary of the Invention", first two paragraphs, and claim 15, col. 17, l. 24-47) each including: a semiconductor feature 303 having a thickness over the insulator, a first surface opposite the insulator (upper main surface of 303) and a sidewall spanning at least a portion of the thickness (sidewall of 303); and a contact layer 318/321 having a first member 318 extending over at least a portion of the first surface and a second member 321 spanning at least a portion of the sidewall; a plurality of dielectric layers 311 and 319 (first and second interlayer dielectric films: col. 7, l. 41-42 and col. 8, l. 30-31) located over the

plurality of microelectronic devices; and a plurality of interconnects 317 extending through ones of the plurality of dielectric layers (namely the dielectric layers with numeral 311 of which can be said that the source lines extends through them, because the source line abuts 317 and extends through its entire thickness) at least one of the plurality of interconnects interconnecting ones of the plurality of microelectronic devices (371 is a source line, inherently interconnecting all source electrodes).

On claim 57: a portion of the semiconductor feature interposes the insulator and the second member of the contact layer (because a straight line can be drawn from a point in the insulator to a point in the second member that intersects the semiconductor feature).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (6,040,589) in view of Lee (US 2001/0023090). As detailed above, Zhang et al anticipate claim 2. Zhang et al do not necessarily teach the further limitation defined by claim 4. However, it would have been obvious to include said further limitation in view of Lee, who teach a crystalline active layer in a thin film transistor (hence analogous art)

(cf. Lee, title, abstract and par. [0043]) to have a thickness between 30 and 1000 Angstroms (A), substantially overlapping the range as claimed (<100 A). Considering the large range said thickness is seen to be a design parameter in light of the Specification of Applicant in which Applicant does not provide an explanation why the difference between the range as claimed (<100 A) and a value such as found in Zhang et al (500 A) is critical to the invention. Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

5. ***Claims 1-2, 5-6, 8-11, 13, 26-28, 30-39, 43-45, 49-52 and 54-58*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuta et al (5,113,234) in view of Zhang et al (6,040,589) and Hillenius (ISBN: 0-471-15237-4). *Furuta et al teach* (title, abstract and Figure 2) a substrate 1; a semiconductor feature 5/9 (col. 2, l. 36-62) located over the substrate and having a thickness, a first (upper main) surface, and a sidewall (wall portion sloping down the sidewall of 5/9) at least a portion of the thickness; and a contact layer 8 (col. 2, l. 53-56) having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the second surface (cf. Figure 2 and col. 2, l. 45-48). With regard to *claim 5*, said contact layer comprises a third member (wall portion on flat lower part of horizontal surface) connected to the second member and interposing a portion of the substrate and a portion of the semiconductor feature (interposing because a straight line can be

drawn between a point of the substrate and a point of the semiconductor feature intersecting with said third member; cf. Figure 2).

Furuta et al do not necessarily teach said substrate to be an insulator resting upon a lower substrate. *However, it would have been obvious to include said insulator in view of Zhang et al,* who teach an insulator 302 as a buried oxide layer (layer that does not reach the upper substrate surface) (*claim 49* is thus met) located over a lower substrate 301 as the essence of silicon-on-insulator (SOI) technology while SOI is well known to reduce parasitic capacitance and thus removes a major obstacle in the down-sizing of transistors: See, for example, *S. J. Hillenius*, "MOSFETs and Related Devices" in "Modern Semiconductor Device Physics", Ed. S.M. Sze, pp. 160-161, John Wiley & Sons, New York (1998) (ISBN: 0-471-15237-4). *Motivation* to include the teaching by Zhang et al, - by which all claim limitations are met, at least derives from the increased device speed resulting from a decrease in parasitic capacitance.

On claim 2: because in Furuta et al a portion of the semiconductor feature interposes the substrate and the second member of the contact layer and in the combined invention the insulator forms the upper portion of the substrate the claim is met in the combined invention.

With regard to *claim 6*, although Furuta et al do not necessarily teach the further limitation of claim 6, Zhang et al teach a thickness of said contact layer is greater than 10 A, namely 500 A (which is the thickness of the titanium substrate portion of 318) (col. 7, l. 50-58). Applicant, in the Specification, does not explain why the claimed range is critical to the invention. Applicant's disclosure does not teach why the range as

claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. *Motivation* for a minimum thickness at least derives from the need to ensure good electrical contact.

With regard to claims 8-11: the contact layer 8 by Furuta et al comprises metal silicide (through polycide) (col. 4, l. 1-2). Furuta et al do not necessarily teach the contact layer to comprise cobalt silicide, nickel silicide or a metal nitride; however, in the Specification the material embodiments of cobalt silicide, nickel silicide and metal nitride are only offered as examples (see par. [0032]: "other conductive materials such as ...NiSi, and CoSi") while one such evidently equivalent material embodiments is taught by Zhang et al, namely: titanium (col. 7, l. 50-58 in Zhang et al). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

With regard to *claim 13*, although Furuta et al do not necessarily teach the further limitation of claim 13, Zhang et al teach a thickness of said contact layer is 500 A (which is the thickness of the titanium substrate portion of 318) (col. 7, l. 50-58). Applicant, in the Specification, does not explain why the claimed range is critical to the invention, and a forteriori not why the difference between the range in the prior art and

the range as claimed is critical to the invention (said difference is at most about 25% of certain values within said claimed range). Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. *Motivation* for a maximum thickness at least derives from the cost considerations involved in providing an adequate electrical contact.

With regard to claims 26 and 45: Furuta et al teach a transistor device (col. 2, l. 28-30), comprising: a substrate 1 (col. 2, l. 31-36); a gate 4 (col. 2, l. 34-41) located over the insulator; source and drain regions 5/9 on opposing sides of the gate and having a thickness over the insulator (cf. Figure 2), each of the source and drain regions having a first surface opposite the substrate (upper main surface) and a sidewall distal from the gate (the wall portion sloping down along 5/9) and spanning at least a portion of the thickness; and source and drain contacts 8 (col. 2, l. 53-56) each having a first member extending over at least a portion of a corresponding first surface (portion abutting the upper horizontal portion of the upper surface of the source and drain regions) and a second member (the portion sloping down along 5/9) spanning at least a portion of a corresponding sidewall (cf. Figure 2 and loc.cit.).

Furuta et al do not necessarily teach the limitation that an insulator located over said substrate such that the gate is located not only over said substrate but also over said insulator (thereby the insulator becomes effectively the upper portion of the

substrate and all limitations are seen to be met in that case). *However, it would have been obvious to include said further limitation in view of Zhang et al,* who teach an insulator 302, in particular an oxide (claim 45) located over a lower substrate 301 as the essence of silicon-on-insulator (SOI) technology while SOI has long been recognized to reduce parasitic capacitance and thus removes a major obstacle in the down-sizing of transistors: see, for example, S. J. Hillenius, "MOSFETs and Related Devices" in "Modern Semiconductor Device Physics", Ed. S.M. Sze, pp. 160-161, John Wiley & Sons, New York (1998) (ISBN: 0-471-15237-4). *Motivation* to include the teaching by Zhang et al, - by which all claim limitations are met, at least derives from the increased device speed resulting from a decrease in parasitic capacitance.

On claim 27: a portion of the semiconductor feature in the combined invention interposes the insulator and the second member of the contact layer (because a straight line can be drawn from a point in the insulator to a point in the second member that intersects the semiconductor feature).

On claim 28: this rejection is provided to the best of examiner's understanding of the intended content of the claim language, which has been noted above to be indefinite. The examiner interprets the claimed "interposing portion" to be a portion of at least one of a drain region and a source region interposing the insulator and the second member. Although Furuta et al do not necessarily teach the further limitation defined by claim 28, it would have been obvious to include said further limitation in view of Zhang et al, who teach the thickness of the source and drain regions, which is the thickness of the active region 303 to be 500 Angstroms, which is at least about 50 Angstroms (col. 6,

l. 55-67). Therefore, the range as claimed is known in the art. Furthermore, Applicant, in the Specification, does not explain why the range as claimed is critical to the invention. Applicant is reminded

On claim 30: said contact layer comprises a third member (wall portion on flat lower part of horizontal surface) connected to the second member and interposing a portion of the substrate and a portion of the semiconductor feature (interposing because a straight line can be drawn between a point of the substrate and a point of the semiconductor feature intersecting with said third member; (cf. Figure 2).

On claim 31: although Furuta et al do not necessarily teach the further limitation of claim 6, Zhang et al teach a thickness of said contact layer is greater than 10 A, namely 500 A (which is the thickness of the titanium substrate portion of 318) (col. 7, l. 50-58). Applicant, in the Specification, does not explain why the claimed range is critical to the invention. Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. *Motivation* for a minimum thickness at least derives from the need to ensure good electrical contact.

On claims 32-36: at least one of the source and drain contacts 8 comprises metal (through polycide, thus teaching claim 32), particularly metal silicide (through polycide, thus teaching claim 33) (col. 4, l. 1-2). Furuta et al do not necessarily teach the contact layer to comprise cobalt silicide, nickel silicide, or a metal nitride as requirement by

claims 34, 35, and 36 respectively. However, in the Specification the material embodiments of cobalt silicide, nickel silicide and metal nitride are only offered as examples (see par. [0032]: "other conductive materials such as ...TiN, TaN, NiSi, and CoSi") while one among such evidently equivalent material embodiments is taught by Zhang et al, namely: titanium (col. 7, l. 50-58 in Zhang et al). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

On claim 37: although Furuta et al do not necessarily teach the further limitation defined by claim 37, it would have been obvious to include said limitation in view of Zhang et al, who teach the inclusion of ITO (indium-tin oxide) in said contact layer so as to function as a pixel electrode (col. 8, l. 38-41). *Motivation* to include the teaching by Zhang et al in this regard derives at least from the optical transparency of ITO, thus making it suitable to function not only as a conductive drain contact but equally well as pixel electrode.

On claim 38: although Furuta et al do not necessarily teach the further limitation defined by claim 38 a similar thickness is taught by Zhang et al, namely 500 Angstroms (col. 7, l. 55-58), which may be interpreted as "less than about" in the absence of a more specific disclosure by Applicant. Furthermore, Applicant, in the Specification, does not explain why the difference between the range of the prior art (including 500 A) and the range as claimed (less than "about" 400 A) is critical to the invention. In view of the

absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

*On claim 39:*at least one of the source and drain regions comprises silicon (col. 2, l. 31-44).

On claims 43 and 44: although Furuta et al do not necessarily teach the further limitation of either claim 43 or claim 44, it would have been obvious to include said further limitations in view of Zhang et al, who teach the source and drain regions, being part of a flat semiconductor feature, to have a thickness of at least about 400 Angstroms (claim 43) and at least about 100 Angstroms (claim 44), namely 500 Angstroms (col. 6, l. 60-67). Considering that the range as found in the prior art is at least motivated by the need to ensure reliable electrical contact there is ample *motivation* to include the teaching by Zhang et al also in this regard.

On claim 45: direct implementation of the teaching by Zhang et al on the insulator meets the claim because the insulator is buried, i.e., nowhere reaches the upperm main surface).

On claims 50-52 and 54-55: The devices of claims 26-28 and 30-31 would necessarily have to be formed in order to function. Claims 50-52 and 54-55 fail to further limit the devices of claims 26-28 and 30-31 other than simply form each of their components.

On claim 56: as explained above under claim 1 (to which we refer for references) a "micro-electronic device comprising an insulator located over a substrate, a semiconductor feature having a thickness over the insulator, a first surface opposite the insulator and a sidewall spanning at least a portion of the thickness, and a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall" as claimed here is unpatentable over Furuta et al in view of Zhang et al and Hillenius. While Furuta et al teach a plurality of dielectric layers 6 and 10 located over the microelectronic device (col. 2, l. 41 and col. 3, l. 6) and a plurality of interconnects 12 extending through ones of the plurality of dielectric layers (col. 3, l. 15-21) Furuta et al do not necessarily teach the further limitations as claimed, i.e., said microelectronic device being one of a plurality of microelectronic devices each so characterized and comprised in an integrated device, at least one of the plurality interconnects interconnecting one of the plurality of microelectronic devices. However, it would have been obvious to include said further limitation ad (a) in view of Zhang et al, who teach the inclusion of a plurality of MOS transistors in an active matrix device (col. 17, l. 24-48), while the very field of invention is defined by Zhang et al as MOS transistors (in particular: thin film transistors) comprised in active matrix liquid crystal display (col. 1, l. 8-14), while at least one of the plurality of interconnects ones of the plurality of microelectronic devices by virtue of being a source line 317 (col. 7, l. 59 – col. 8, l. 30 and Figure 2). Inclusion of the teaching by Zhang et al in the invention by Furuta et al thus constitutes nothing more

than an obvious application of the invention by Furuta et al, rendering the invention more profitable. Increased profitability constitutes motivation.

On claims 57-58: as the further limitations of claims 57 and 58 were seen to be met by the individual microelectronic devices in the combined invention by Furuta et al, Zhang et al and Hillenius (see claims 2 and 5) these limitations are necessarily met in the combined invention of the integrated circuit device as well.

6. ***Claims 9-11 and 13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (6,040,589). As detailed above, Zhang et al anticipate claim 1. Although Zhang et al do not necessarily teach the contact layer to comprise of cobalt silicide, nickel silicide, or of metal nitride, it would have been obvious to include the further limitations of claims 9, 10, and 11 in view of the mere disclosure by Applicant of cobalt silicide, nickel silicide or metal nitride as examples evidently equivalent to titanium, which is comprised in the contact layer by Zhang et al (see paragraph [0032] on page 8 of the Specification and see Zhang et al, col. 7, l. 50-62). Applicant is reminded that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

With regard to claim 13, although Zhang et al do not necessarily teach the further limitation as defined by claim 13, Zhang et al teach a thickness of said contact layer is 500 A (which is the thickness of the titanium substrate portion of 318) (col. 7, l. 50-58). Applicant, in the Specification, does not explain why the claimed range is critical to the

invention, and a forteriori not why the difference between the range in the prior art and the range as claimed is critical to the invention (said difference is at most about 25% of certain values within said claimed range). Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. *Motivation* for a maximum thickness at least derives from the cost considerations involved in providing an adequate electrical contact.

7. ***Claims 15-17*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (6,040,589) in view of Morita et al (WO-2002/82526) (for the latter Morita et al (US 2004/0142579 A1) shall be used as translation, said WO publication being the publication of the PCT of which US 2004/0142579 is the patent application of the national stage thereof). Zhang et al anticipate claim 1, as detailed above. *Zhang et al do not necessarily teach* the further limitation as defined by either of claims 15, 16 or 17. However, it would have been obvious to include said further limitations in view of Morita et al, who teach the semiconductor thin film in a thin film transistor (hence analogous art) to comprise silicon, germanium and carbon (see par. [0175]) so as to enable simultaneous use of a p-channel and an n-channel region. At least for reasons of compactness of the device there is ample *motivation* to include the teaching by Morita et al in the invention by Zhang et al.

8. ***Claims 21-23*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al in view of Asami et al (US 2002/0014625 A1). As detailed above, Zhang et al anticipate claim 1. Zhang et al do not necessarily teach the further limitation as defined by claims 21 or 22. However, it would have been obvious to include said further limitations in view of Asami et al, who, in a patent application on a thin film transistor (hence analogous art) teach the insulator to comprise silicon oxide, silicon nitride, silicon oxynitride or the like (see par. [0052]) as barriers against alkaline metal migration from the glass substrate. Note also in Zhang et al the substrate is made of glass. The prior art thus shows substantial equivalence of silicon oxide, silicon nitride and silicon oxynitride as material selections of the insulator by Zhang et al. Note that Zhang et al teach silicon oxide (col. 6, l. 60-62). Applicant, in the disclosure, does not explain why the material selection as claimed in claim 21 or claim 22 is critical to the invention. Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

With regard to claim 23, silicon nitride as taught by Asami et al has a dielectric constant (about 7.5) that is higher than that of silicon dioxide (about 3.9). No specific criterion is provided in the Specification to define what is meant by "high" in the wording "high-k dielectric constant". Within the context of the rejection under 35 U.S.C. 112, second paragraph, due to the indefiniteness introduced by the relative concept of "high" in "high-k dielectric constant", a rejection must be made over the art cited under the

assumption that "high" means "higher than the dielectric constant of silicon dioxide": the Specification merely lists a number of possible material embodiments that includes silicon nitride; silicon nitride has indeed a dielectric constant higher than that of silicon dioxide.

9. ***Claims 29 and 53*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Furita et al, Zhang et al and Hillenius as applied to claim 26 above, and further in view of Lee (US 2001/0023090). *Neither Furita et al, nor Zhang et al, nor Hillenius necessarily teach the further limitation as defined by claim 29. However, it would have been obvious to include said further limitation in view of Lee,* who teach a crystalline active layer in a thin film transistor (hence analogous art) (cf. Lee, title, abstract and par. [0043]) to have a thickness between 30 and 1000 Angstroms (A), substantially overlapping the range as claimed (<100 A). Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. With regard to *claim 53*, the device of claim 29 would necessarily have to be formed in order to function. Claim 53 fails to further limit the device of claim 29 other than simply form each of their components.

10. ***Claims 40-42*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Furita et al, Zhang et al and Hillenius as applied to claim 26, and further in view of Morita et al (WO-2002/82526) (for the latter Morita et al (US 2004/0142579 A1) shall be

used as translation, said WO publication being the publication of the PCT of which US 2004/0142579 is the patent application of the national stage thereof). Zhang et al anticipate claim 1, as detailed above. *Zhang et al do not necessarily teach* the further limitation as defined by either of claims 40, 41 or 42. However, it would have been obvious to include said further limitations in view of Morita et al, who teach the semiconductor thin film in a thin film transistor (hence analogous art) to comprise silicon, germanium and carbon (see par. [0175]) so as to enable simultaneous use of a p-channel and an n-channel region. At least for reasons of compactness of the device there is ample *motivation* to include the teaching by Morita et al in the invention by Zhang et al.

11. ***Claims 45-48*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Furita et al, Zhang et al and Hillenius as applied to claim 26, in further in view of Asami et al (US 2002/0014625 A1). Furita et al do not necessarily teach the further limitation as defined by claims 45, 46 or 47. However, it would have been obvious to include said further limitations in view of Asami et al, who, in a patent application on a thin film transistor (hence analogous art) teach the insulator to comprise silicon oxide, silicon nitride, silicon oxynitride or the like (see par. [0052]) which, by virtue of the higher dielectric constant of silicon nitride and silicon oxynitride in comparison with silicon dioxide is at least motivated by the resulting further decrease of the parasitic capacitance. Furthermore, Applicant, in the disclosure, does not explain why the material selection as claimed in claims 45, 46 or 47 is critical to the invention. Applicant is reminded in this regard that it has been held that mere selection of known materials

generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. With regard to *claim 48*, silicon nitride as taught by Asami et al has a dielectric constant (about 7.5) that is higher than that of silicon dioxide (about 3.9). No specific criterion is provided in the Specification to define what is meant by "high" in the wording "high-k dielectric constant". Within the context of the rejection under 35 U.S.C. 112, second paragraph, due to the indefiniteness introduced by the relative concept of "high" in "high-k dielectric constant", a rejection must be made over the art cited under the assumption that "high" means "higher than the dielectric constant of silicon dioxide": the Specification merely lists a number of possible material embodiments that includes silicon nitride; silicon nitride and silicon oxynitride have indeed a dielectric constant higher than that of silicon dioxide (> about 7 rather than about 3.9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
March 18, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826).